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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,550	12/29/2000	Ritesh Trivedi	42390P10725	1451

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EXAMINER
MAI, SON LUU

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/752,550	TRIVEDI ET AL.
	Examiner	Art Unit
	Son L. Mai	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continu d Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10-29-2002 has been entered.

2. The Amendment filed on 10-29-2002 has been entered. Accordingly, Claims 46-67 are pending and presented for examination.

Information Disclosure Statement

3. The Information Disclosure Statement filed on 07-19-2002 has been considered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 59 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In lines 1-2, an article "the" should be added before "semiconductor device" since the device has been mentioned in claim 55.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 46, 48-55, and 57-60 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,959,919 issued to Choi.

Regarding claim 46, Choi teaches a method comprising: receiving a signal pulse (EQ in fig. 2); and in response to the signal pulse: pulling a voltage of a first drain bias circuit (right side of sense amplifier 26) for a non-volatile memory cell (23) to a voltage potential (Vcc) of a voltage source; pulling a voltage of a second drain bias circuit (left side of sense amplifier 26) of a reference cell (21) to the voltage potential of the voltage source; and shorting a sense node (on bit line 24) for the non-volatile memory cell to a reference node (on dummy line 22) for the reference cell (when transistor MN26 is on).

Regarding claim 48, Choi further teaches the step of pulling the voltage of the first drain bias circuit to the voltage potential of the voltage source comprises enabling a first kicker device (MP24) coupled to the first drain bias circuit; and pulling the voltage of

the second drain bias circuit to the voltage potential of the voltage source comprises enabling a second kicker device (MP21) coupled to the second drain bias circuit.

Regarding claim 49, Choi shows in figure 2 that the first kicker device MP24 and the second kicker device MP21 are high performance transistors.

Regarding claim 50, Choi teaches shorting the sense node (on bit line 24) to the reference node (on dummy line 22) comprises enabling a semiconductor device (MN26) coupled between the sense node and the reference node.

Regarding claim 51, at column 1, line 58 through column 2, line 7, Choi describes that enabling the semiconductor device (MN26) coupled between the sense node and the reference node equalizes a voltage potential of the sense node with a voltage potential of the reference node during bit charging.

Regarding claim 52, Choi shows that when transistors MP21 and MP24 are on, pulling the voltage potential of the sense node to the voltage potential of the voltage source minus the voltage across the first drain bias circuit (Vcc minus threshold voltage of transistor MP25); and pulling the voltage potential of the reference node to the voltage potential of the voltage source minus the voltage across the second drain bias circuit (Vcc minus threshold voltage of transistor MP22).

Regarding claim 53, Choi teaches at column 2, lines 5-19, the signal pulse (EQ) is received prior to sensing the contents of the non-volatile memory cell.

Regarding claim 54, Choi's figure 2 shows the first drain bias circuit and the second drain bias circuit, each comprises a cascode amplifier (MN25 and MN24).

Regarding claim 55, Choi teaches a non-volatile memory device comprising: a first kicker device (MP24 in figure 2), a first terminal of the first kicker device being coupled to a voltage source and a second terminal of the first kicker device being coupled to a first drain bias circuit (right side of sense amplifier 26) for a memory cell (23) of the non-volatile memory device; a second kicker device (MP21), a first terminal of the second kicker device being coupled to the voltage source and a second terminal of the second kicker device being coupled to a second drain bias circuit (left side of sense amplifier 26) for a reference cell (21) of the non-volatile memory device; and a semiconductor device (MN26), a first terminal of the semiconductor device being coupled to a sense node (on bit line 24) of the memory cell and a second terminal of the semiconductor device being coupled to a reference node (on dummy line 22) of the reference cell; in response to a signal pulse (EQ): the first kicker device (MP24) pulling a voltage of the first drain bias circuit to a voltage potential (Vcc) of the voltage source, the second kicker device (MP21) pulling a voltage of the second drain bias circuit to the voltage potential of the voltage source, and the semiconductor device (MN26) shorting the sense node with the reference node.

Regarding claim 57, Choi teaches at column 2, lines 5-19, the signal pulse (EQ) is received prior to sensing the contents of the non-volatile memory cell.

Regarding claim 58, Choi shows in figure 2 that the first kicker device MP24 and the second kicker device MP21 are high performance transistors

Regarding claim 59, at column 1, line 58 through column 2, line 7, Choi describes that the semiconductor device (MN26) equalizes a voltage potential of the sense node with a voltage potential of the reference node during bit charging.

Regarding claim 60, Choi's figure 2 shows the first drain bias circuit and the second drain bias circuit each comprises a cascode amplifier (MN25 and MN24).

8. Claims 47, 56, 61-67 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,038,173 issued to Yero.

Regarding claim 61, Yero teaches a flash memory device (column 1, line 9), comprising: a memory cell array (connected to bit line LB); a reference cell array (connected to reference line LR); a first drain bias circuit (connected to LB) for a memory cell in the memory cell array and a second drain bias circuit (connected to LR) for a reference cell in the reference cell array; a first kicker device (T7), a first terminal of the first kicker device being coupled to a voltage source (Vcc) and a second terminal of the first kicker device being coupled to the first drain bias circuit; a second kicker device (T8), a first terminal of the second kicker device being coupled to the voltage source and a second terminal of the kicker device being coupled to the second drain bias circuit; and a semiconductor device (T13), a first terminal of the semiconductor device being coupled to a sense node of the memory cell and a second terminal of the semiconductor device being coupled to a reference node of the reference cell; upon receiving an enable signal (output signal of inverter gate INV3): the first kicker device T7 pulls a voltage of the first drain bias circuit to a voltage potential of the voltage

source, the second kicker device T8 pulls a voltage of the second drain bias circuit to the voltage potential of the voltage source, and the semiconductor device T13 shorts the sense node with the reference node.

Regarding claim 62, Yero teaches the enable signal (from inverter INV3) is received during a precharging step prior to sensing the contents of the memory cell (column 4, lines 46-60).

Regarding claims 63 and 64, Yero teaches the first kicker device T7 and the second kicker device T8 are P-channel high performance transistors

Regarding claim 65, Yero teaches that the semiconductor device T13 equalizes a voltage potential of the sense node with a voltage potential of the reference node during bit charging (column 4, lines 55-60).

Regarding claim 66, Yero shows in figure 1, the first drain bias circuit and the second drain bias circuit each comprise a cascode amplifier (T1 and T2).

Regarding claim 67, Yero teaches an apparatus comprising: means (T7) for pulling a voltage of a first drain bias circuit for a non-volatile memory cell to a voltage potential (Vcc) of a voltage source in response to an enable signal (from inverter INV3); means (T8) for pulling a voltage of a second drain bias circuit for a reference memory cell to the voltage potential of the voltage source in response to the enable signal; and means (T13) for shorting a sense node of the non-volatile memory cell to a reference node of the reference cell in response to the enable signal.

Regarding claims 47 and 56, Yero teaches that the non-volatile memory cell comprises a flash memory cell (column 1, line 9).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee (U.S. Patent 5,804,992) teaches an equalizing circuit connecting between input terminals of a sense amplifier for equalizing a potential of the terminals before reading mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 305-3497. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 308-7724 for regular communications and 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-0956.

01-08-2003

Son L. Mai
Primary Examiner
Art Unit 2818